SPECIFICATION FOR TFT LCD MODULE
TFT 模组规格书

Part NO. 产品型号	SJ-QV28-0548-A0
SIZE 尺寸(英寸)	2.8
Customer 客户名称	
Customer Part NO. 客户型号	
Date 日期	2019-11-1

SCJ Approval
双创嘉确认

Designed by 设计	Checked by 审核	Approved by 确认
		周冬华

Customer Approval
客户确认

Designed by 核准	Checked by 审核	Approved by 确认
备注 Note	☐ Approve Specification Only	
	☐ Approve Specification and Sample	

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Records Of Revision

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NO. 序号	Version 版本	Description 描述	Date 日期	Note 备注
1	A	Original	2019-11-1	
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1. Introduction

1.1 Scope of application

This specification applies to the Negative type TFT transmissive dot matrix LCD module that is supplied by SHENZHEN SHENGJI PHOTOELECTRIC. CO., LTD.

This LCD module should be designed for mobile phone use.LCD specification:6:00, Dots 240xRGBx320.As to basic specification of the driver IC, refer to the IC (GC9306) specification and datasheet.

This specification applies to the Negative type TFT transmissive dot matrix LCD module that is supplied by SHENZHEN SHENGJI PHOTOELECTRIC. CO., LTD.

1.2 Structure:

Double display structure:

TFT Module + FPC + BL

FULL 262k Color 2.4 inch TFT LCD size for main LCD;

One bare chip with gold bump (COG) TECH;

1.3 TFT features:

Structure: TFT PANNEL+IC+FPC;

Transmissive Type LCD

240 dot-source and 320 dot-gate outputs;

262k Color;

White LED back light;

1.4 Applications:

Mobile; phone;Mp4.

1.5 This module uses ROHS material

2. General Specification

No.	ITEM	Standard value	UNIT
1	LCD size	2.8	Inch
2	Number of Dots	240*(RGB)*320	Dots
3	Display Area	43.2(W)*57.6(H)	mm
4	Module Size(W*H*T)	50(W)*69.26(H)*2.2(T)	mm
5	LCD Type	TFT Negative Transmissive	/
6	Driver element	a-Si TFT Active matrix	/
7	Pixel Arrangement	RGB Vertical Stripe	/
8	Pixel Pitch (W*H)	0.18(H)*0.18(V)um	um
9	Viewing Direction	12 o'clock(Gray inversion)	/
10	Driver IC	GC9306	/
11	Interface	16-bit Parallel Interface	/
12	Back Light	White LED	
13	Touch Panel Type	/	
14	Approx. Weight	/	g

3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	VDD	-0.3	**4.6**	70
Input voltage for logic	VIN	-0.3	**4.6**	80
Supply current (One LED)	ILED	/	**30**	3.3
Operating temperature	TOP	-20	**70**	3.3
Storage temperature	TST	-30	**80**	0.1

4. Elecctrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Applicable terminal
Supply voltage for logic	VDD	2.4	2.75	3.3	V	Operating voltage
Interface Operation Voltage	VDDI	1.65	1.8	3.3	V	I/O Supply Voltage
Logic-Low Input Voltage	VIL	VSS	-	0.3VDDI	V	
Logic-High Input Voltage	VIH	0.7VDDI	-	VDDI	V	
Input leakage current	IIL	-0.1	-	0.1	μA	
LED Forward voltage	Vf	2.8	3.0	3.3	V	--

Input backlight current	ILED	-	80	-	mA	--

5.Optical Characteristices

ITEM		SYMBOL	CONDITIONS	SPECIFICATIONS			UNIT	NOTE
				MIN.	TYP.	MAX		
Brightness		B		--	200	--	cd/m2	Note 1
Uniformity		Un		80	85		%	Note 2
Response Time(By Quick)		Tr+Tf	θ = 0°	-	25	40	ms	Note 5
Contrast Ratio		CR	θ = 0°	350	500	--	--	Note 4
Viewing Angle	Horizontal	θ 3	CR>=10	40	45	--	Deg.	Note 3
		θ 9	CR>=10	40	45	--		
	Vertical.	θ 12	CR>=10	45	50	--		
		θ 6	CR>=10	15	20			
Color chromaticity (CF only with ITO, light source is C light, CIE 1931)	White	Wx	θ = 0°	0.284	0.299	0.314		Note 4
		Wy		0.318	0.333	0.348		
	Red	Rx		0.611	0.626	0.641		
		Ry		0.317	0.332	0.347		
	Green	Gx		0.267	0.282	0.297		
		Gy		0.574	0.589	0.604		
	Blue	Bx		0.122	0.137	0.152		
		By		0.134	0.149	0.164		
NTSC				55	60		%	Note 5

Note 1:Test condition is:

(1) Center point on active area.

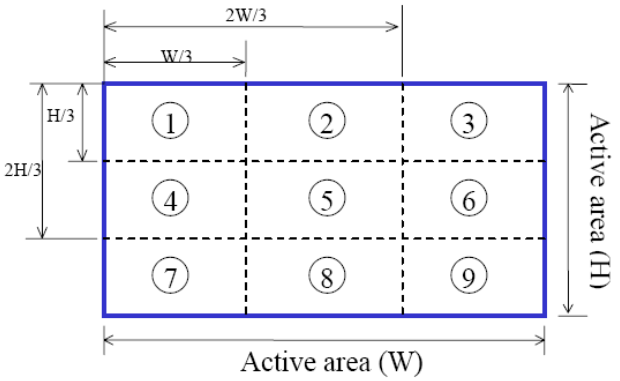
(2)Best Contrast.

Note 2:Uniform measure condition:

(1)Measure 9 point. Measure location show below;

(2)Uniform=(Min. brightness /Max. brightness)*100%

(3)Best Contrast.



Note:

3.Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o' clock direction and the vertical or 6, 12 o' clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.2).

4.Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIG.2) Luminance Contrast Ratio (CR) is defined mathematically.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

5. The electro-optical response time measurements shall be made as FIG.3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tfand 90% to 10% isTr.

Figure 1. The definition of Vth & Vsat

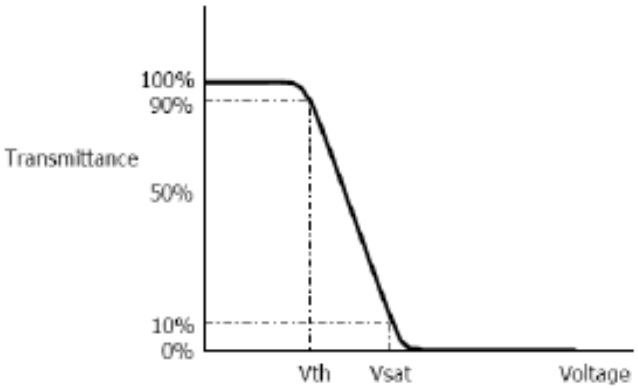


Figure 2. Measurement Set Up

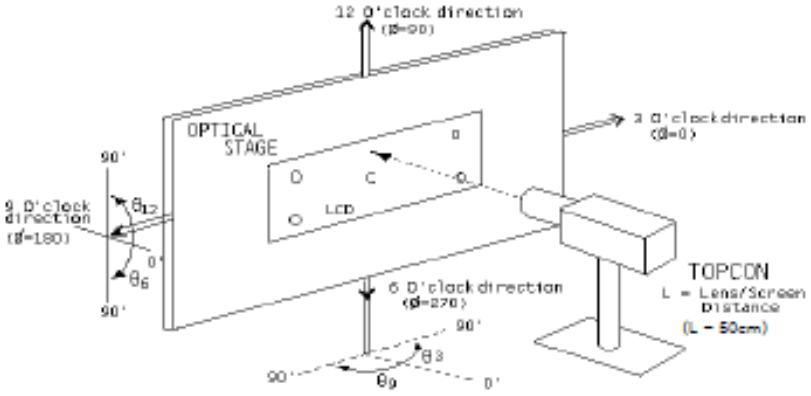
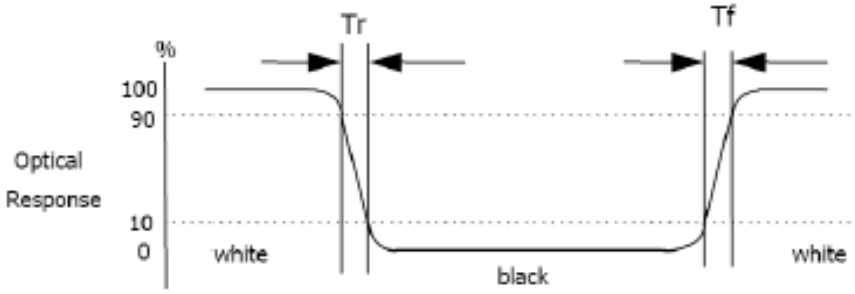


Figure 3. Response Time Testing



6. Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec

after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after

RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out

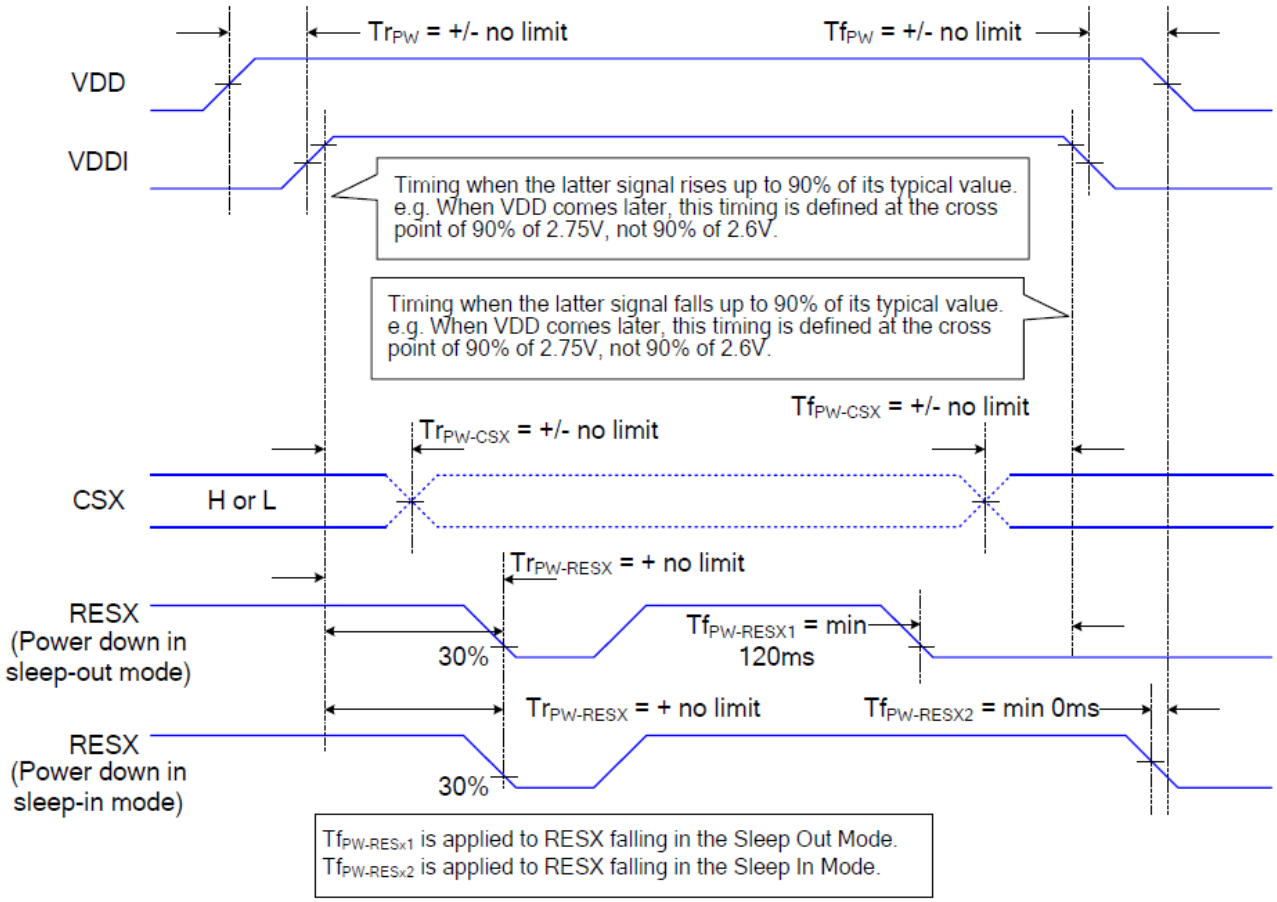
command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to

apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not

guaranteed.

6.1The power on/off sequence is illustrated below



6.2 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off

sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the

display (blank display) and remains blank until “Power On Sequence” powers it up.

7. 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus:

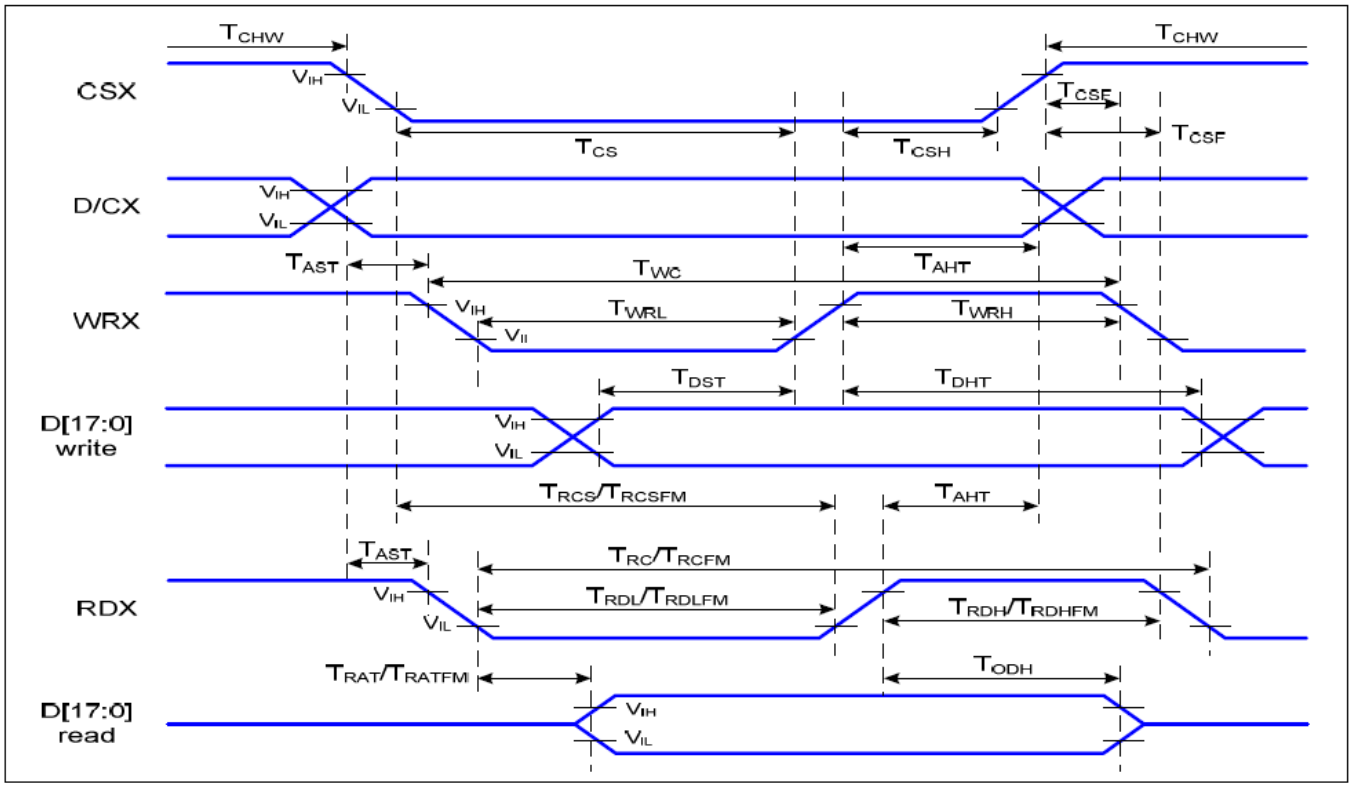


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse “H” duration	15		ns	
	T_{WRL}	Control pulse “L” duration	15		ns	

RDX (ID)	TRC	Read cycle (ID)	160		ns	-read command & data ram
	TRDH	Control pulse “H” duration (ID)	90		ns	
	TRDL	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	TRCFM	Read cycle (FM)	450		ns	When read ID data
	TRCFM	Control pulse “H” duration (FM)	90		ns	
	TRDLFM	Control pulse “L” duration (FM)	355		ns	
RDX (FM)	TRCFM	Read cycle (FM)	450		ns	When read from frame memory
	TRCFM	Control pulse “H” duration (FM)	90		ns	
	TRDLFM	Control pulse “H” duration (FM)	355		ns	
D[17:0]	TDST	Data setup time	10		ns	For CL=30pF
	TDHT	Data hold time	10		ns	
	TRAT	Read access time (ID)		40	ns	
	TRATFM	Read access time (FM)		340	ns	
	TODH	Output disable time	20	80	ns	

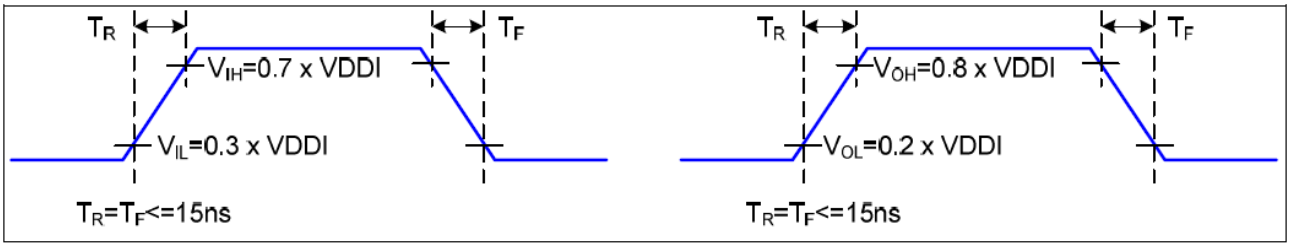


Figure 2 Rising and Falling Timing for I/O Signal

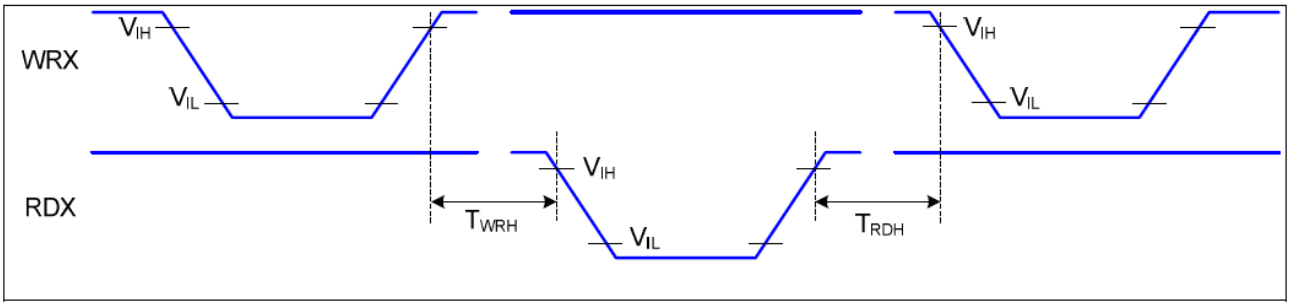


Figure 3 Write-to-Read and Read-to-Write Timing

8. MCU Interface Pin Function

NO.	SYMBOL	Description	I/O
1	VCC	Power Supply for Analog, Digital System and Booster Circuit.	I
2	GND	System Ground	I
3	BL_A	Anode of Backlight (2.8V-3.2V Typical:3 V)	I
4	/RESET	This signal will reset the device and it must be applied to properly initialize the chip.Signal is active low.	I
5	/CS	Chip selection pin。 (Low enable.; High disable.)	I
6	RS	Display data/command selection pin in parallel interface.	I
7	WR	Write enable in MCU parallel interface.	I
8	RD	Read enable in 8080 MCU parallel interface.	I
9	DB0	Data bus.NO.0	I/O
10	DB1	Data bus.NO.1	I/O
11	DB2	Data bus.NO.2	I/O
12	DB3	Data bus.NO.3	I/O
13	DB4	Data bus.NO.4	I/O
14	DB5	Data bus.NO.5	I/O
15	DB6	Data bus.NO.6	I/O
16	DB7	Data bus.NO.7	I/O
17	DB8	Data bus.NO.8	I/O
18	DB9	Data bus.NO.9	I/O
19	DB10	Data bus.NO.10	I/O
20	DB11	Data bus.NO.11	I/O
21	DB12	Data bus.NO.12	I/O
22	DB13	Data bus.NO.13	I/O
23	DB14	Data bus.NO.14	I/O

24	DB15	Data bus.NO.15	I/O

9.Mechanical drawing